VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims

The claims have been amended as follows:

21. (Twice Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and uncurved peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that provides the bottom surface and is non-transparent, and the second housing portion contacts the upper surface, **is farther from the bottom surface than the lower surface is from the bottom surface,** provides at least a portion of the top surface and is transparent; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

31. (Twice Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface, contacts the lower surface and the outer side surfaces, is spaced from the light sensitive cell and is non-transparent, and the second housing portion is a single-piece or double-piece that provides a central portion of the top surface within the peripheral portion of the top surface, contacts the first housing portion, the light sensitive cell and the conductive trace, is spaced from

the lower surface, **is farther from the bottom surface than the lower surface is from the bottom surface,** is transparent and is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

61. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that **contacts the chip,** covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

66. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that **contacts the chip,** covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing, is bent outside the insulative housing and is electrically connected to the pad inside the insulative housing.

71. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that **contacts the chip,** covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing, does not contact an insulative material outside the first housing portion and is electrically connected to the pad inside the insulative housing.

76. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that **includes a lead and a planar metal trace, wherein the lead** extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, **and the planar** ~~wherein the conductive trace includes a plated~~ metal trace **contacts and is not integral with the lead,** ~~that~~ extends across one of the side surfaces and does not extend outside the insulative housing.

81. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that **includes a lead and a planar metal trace, wherein the lead** extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, **and the planar** ~~wherein the conductive trace includes a plated~~ metal trace ~~that~~ **contacts and is not integral with the lead,** contacts the first and second housing portions, extends across one of the side surfaces and does not extend outside the insulative housing.

86. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that **includes a lead and a planar metal trace, wherein the lead** extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, **and the planar** ~~wherein the conductive trace includes a plated~~ metal trace ~~that~~ **contacts and is not integral with the lead,** contacts the first and second housing portions, overlaps the pad, extends across one of the side surfaces and does not extend outside the insulative housing.

91. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that **contacts the chip,** covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, and the top surface is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

96. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that **contacts the chip,** covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

101. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that **contacts the chip,** covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the central portion of the top surface is recessed relative to the peripheral portion of the top surface, and the top surface is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

106. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that **contacts the chip,** covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the central portion of the top surface is recessed relative to the peripheral portion of the top surface, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

111. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that **contacts the chip,** covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, and the top, bottom and peripheral side surfaces are exposed; and

a conductive trace that extends outside the insulative housing, is located between the second housing portion and the chip inside the insulative housing, is spaced from the top surface and is electrically connected to the pad inside the insulative housing.

116. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that **contacts the chip,** covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive

cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, and the top, bottom and peripheral side surfaces are exposed; and

a conductive trace that extends outside the insulative housing, includes a top surface that faces away from the chip and contacts the second housing portion inside the insulative housing, includes a bottom surface that faces towards the chip and contacts the second housing portion inside the insulative housing, is spaced from the top and bottom surfaces, extends through one of the peripheral side surfaces and is electrically connected to the pad inside the insulative housing.

121. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion is located within and recessed relative to the peripheral ledge, contacts the light sensitive cell, **does not extend midway between the upper and lower surfaces outside the chip** and is transparent; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

126. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that includes a top surface, a bottom surface, peripheral

side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, the second housing portion is located within and recessed relative to the peripheral ledge, contacts the light sensitive cell, **does not extend midway between the upper and lower surfaces outside the chip** and is transparent, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

131. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion is located within and recessed relative to the peripheral ledge, contacts the light sensitive cell and the inner side surfaces, **does not extend midway between the upper and lower surfaces outside the chip** and is transparent; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

136. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, the second housing portion is located within and recessed relative to the peripheral ledge, contacts the light sensitive cell and the inner side surfaces, **does not extend midway between the upper and lower surfaces outside the chip** and is transparent, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

141. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, uncurved peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and ~~uncurved~~ inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion **extends into** ~~is located within and recessed relative to~~ the peripheral

ledge, contacts the light sensitive cell, **does not extend midway between the upper and lower surfaces outside the chip** and is transparent; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

146. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, uncurved peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and ~~uncurved~~ inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, the second housing portion **extends into** ~~is located within and recessed relative to~~ the peripheral ledge, contacts the light sensitive cell, **does not extend midway between the upper and lower surfaces outside the chip** and is transparent, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

REMARKS

Claim 1-150 are pending. In this Supplemental Response, claims 31, 41, 61, 66, 71, 76, 81, 86, 91, 96, 101, 106, 111, 116, 121, 126, 131, 136, 141 and 146 have been amended. No new matter has been added.

The application is believed to be in condition for allowance. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 1, 2003.

D Sigmond — 5/1/03

David M. Sigmond — Date of Signature
Attorney for Applicant

Respectfully submitted,

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